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AMENDMENTS TO THE CLAIMS

1-7. (Canceled)

8. (Currently Amended) ~~[[The]]~~ A processor ~~of claim 7~~ comprising:

a plurality of pipeline stages to perform an inner loop of a hash algorithm, the plurality of pipeline stages comprising at least as many pipeline stages as there are iterations of the inner loop to be performed and as many pipeline stages as there are chaining variables to be used in the inner loop, wherein each iteration of the inner loop is performed by a dedicated pipeline stage, each pipeline stage comprises an adder, a shifter, and logic to perform a function, and the plurality of pipeline stages comprises 88 pipeline stages to process 512 bits of data, and

control logic to schedule operations to be executed within the plurality of pipeline stages, wherein operations are to be scheduled by the control logic and executed by the plurality of pipeline stages so as to minimize data dependencies between iterations of the inner loop to be performed,

wherein the hash algorithm is chosen from a group of secure hash algorithms (SHA) consisting of SHA-1, SHA-128, SHA-196, SHA-256, and message digest 5 (MD5), and is to be performed at an operating frequency equal to that of the adder.

9-14. (Canceled)

15. (Original) A machine-readable medium having stored thereon a set of instructions, which if executed by a machine cause the machine to perform a method

42390P14932

PATENT

comprising:

performing a plurality of iterations of an inner loop of an hash algorithm in parallel, the plurality of iterations performed in parallel being limited, at least in part, by dependencies between each of the plurality of iterations of the inner loop;

adding initial values of a plurality of chaining variables to final values of the plurality of chaining variables, the final values being a result of performing the plurality of iterations of the inner loop.

16. (Previously Presented) The machine-readable medium of claim 15 wherein the method further comprises controlling scheduling of operations performed as a result of performing the plurality of iterations of the inner loop, the scheduling being controlled so as to minimize a critical path among the operations.

17. (Original) The machine-readable medium of claim 16 wherein the critical path depends upon the dependencies between the plurality of iterations of the inner loop.

18. (Original) The machine-readable medium of claim 17 wherein the method further comprises decoding the inner loop of the hash algorithm into a first number of operational stages, the first number of operational stages being equal to at least the plurality of iterations.

19. (Original) The machine-readable medium of claim 18 wherein the inner loop is to be performed to process a first number of data elements transmitted over a network.

42390P14932

PATENT

20. (Original) ~~[[The]]~~ A machine-readable medium of ~~claim 19 wherein~~ having stored thereon a set of instructions, which if executed by a machine cause the machine to perform a method comprising:

performing a plurality of iterations of an inner loop of an hash algorithm in parallel, the plurality of iterations performed in parallel being limited, at least in part, by dependencies between each of the plurality of iterations of the inner loop;

adding initial values of a plurality of chaining variables to final values of the plurality of chaining variables, the final values being a result of performing the plurality of iterations of the inner loop;

controlling scheduling of operations performed as a result of performing the plurality of iterations of the inner loop, the scheduling being controlled so as to minimize a critical path among the operations, wherein the critical path depends upon the dependencies between the plurality of iterations of the inner loop;

decoding the inner loop of the hash algorithm into a first number of operational stages, the first number of operational stages being equal to at least the plurality of iterations, wherein the inner loop is to be performed to process a first number of data elements transmitted over a network, and the first number of operational stages is at least 83 and the first number of data elements comprises 512 bits.

21-41. (Canceled)